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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/891,466	06/27/2001	David S. Dunning	2207/11266	1394

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EXAMINER	
NGUYEN, LINH M	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 10/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/891,466	DUNNING ET AL.	
	Examiner	Art Unit	
	Linh M. Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 June 2001 and 18 April 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *10-22* is/are allowed.

6)☒ Claim(s) *1,2,5,7 and 9* is/are rejected.

7)☒ Claim(s) *3,4,6 and 8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *04/18/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-22 are presented in the instant application according to the Applicants' filing on 06/27/2001.

Inventorship

1. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-2, 5, 7 and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by, Dally and Poulton, Digital Systems Engineering, Figs. 12-50 and 12-51 (of record).

With respect to claim 1, Dally et al. discloses, in Fig. 12-51(b), a phase interpolator, to interpolate between a plurality of clock phases comprising a) a plurality of switching legs *(first one coupled to (Da,Da') and second one coupled to (Db, Db')* coupled to a common output [I, I'], each including a pair of differential switching transistors [(Da,Da'), (Db,Db')] each having a gate and two additional terminals, one of which is coupled to the common output, the gates coupled to a respective one of the plurality of clock phases and its complement; a tail [(k3,k2,k1,k0); (k3',k2',k1',k0')] coupling the other terminal of the switching transistors to ground, the tail made up of a plurality of transistors; and b) a load *(resistors)* coupling the common output to a voltage.

With respect to claim 2, Dally et al. discloses, in Fig. 12-51(b), that the plurality of clock phases comprises four phases [Da, Da', Db, Db'].

With respect to claim 5, Dally et al. discloses, in Fig. 12-51(b), that the plurality of clock phases include all phases needed for every phase of interpolation.

With respect to claim 7, Dally et al. discloses, in Fig. 12-51(b) and pp. 605, 2nd paragraph, that the switching transistors are of large enough size to reject some common mode noise due to charge injection at nodes between the tail and switching transistors.

With respect to claim 9, Dally et al. discloses, in Fig. 12-51(b) and pp. 605, 2nd paragraph, that the load is provided by load transistors and the load transistors and the tail transistors are selected to be of a size to reduce the interpolator output to very small signals.

Allowable Subject Matter

5. Claims 10-22 are allowed.

6. Claims 3-4, 6 and 8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. The following is a statement of reasons for the indication of allowable subject matter:

The closest prior art on record does not show or fairly suggest

a) A phase interpolator, in which each of the tails comprises four transistors in parallel to make available 16 phases of the reference clock and its complement, as called for in claim 3;

b) A phase interpolator including an N bit digital control, where N equals the total number of transistors in tails, the digital control having N outputs coupled to respective gates in the transistors in the tails, as called for in claim 4;

c) A phase interpolator, in which switching transistors are large enough to load the input clocks such that they have a rise and fall times that are equal to or larger than one quarter of an input clock period, as called for in claim 8.

d) A phase interpolator, to interpolate between four input clock phase signals having four switching legs, each including a pair of differential switching transistors each having a gate, the respective gates coupled respective ones of a plurality of clock phases and their complements, each differential switching transistors coupled to a respective one of the common output line and the common complemented output line, in combination with the remaining claimed limitations as called for in claim 10; and

e) A tracking receiver, in which a remote clock recovery mechanism including an N bit digital control, where N equals the total number of transistors in the tails, the control receiving a control input from the phase and frequency having N outputs coupled to respective gates in the transistors in the tails, in combination with the remaining claimed limitations, as called for in claim 16.

Citation of Relevant Prior Art

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Prior art Chen (U.S. Patent No. 6,359,486) discloses a modified phase interpolator and method to use same in high-speed, low power applications.

Prior art Garlepp et al. (U.S. Patent No. 6,133,773) discloses a method and apparatus for an adjustable phase interpolator.

Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh M. Nguyen whose telephone number is (571) 272-1749. The examiner can normally be reached on Alternate Fri, Monday - Thursday from 7:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Linh M. Nguyen
Primary Examiner
Art Unit 2816

LMN

LINH MY NGUYEN
PRIMARY EXAMINER